# TRANSMITTAL FORM

*(to be used for all correspondence after initial filing)*

| | |
|---|---|
| **Application Number** | 09/578,895 |
| **Filing Date** | May 26, 2000 |
| **First Named Inventor** | Shunpei YAMAZAKI et al. |
| Group Art Unit | 2811 |
| Examiner Name | Gene M. Munson |
| Total Number of Pages in This Submission | |
| Attorney Docket Number | 740756-2160 |

## ENCLOSURES *(check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment / Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers *(for an Application)*
- [ ] Drawing(s)
- [ ] Declaration and Power of Attorney
- [ ] Licensing-related Papers
- [x] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Application Data Sheet
- [ ] Request for Corrected Filing Receipt with Enclosures
- [ ] A self-addressed prepaid postcard for acknowledging receipt
- [ ] Other Enclosure(s) (*please identify below*):

Remarks

[x] The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 19-2380 (740756-2160) for the above identified docket number.

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

| | |
|---|---|
| Firm *or* Individual name | Jeffrey L. Costellia, Reg. No. 35,483<br>Nixon Peabody LLP<br>401 9th Street, N.W.<br>Suite 900<br>Washington, D.C. 20004-2128 |
| Signature | |
| Date | September 5, 2003 |

## CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]

I hereby certify that this correspondence is being:

- [ ] deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop _____, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450
- [ ] transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (703) _____.

_____ Date

_____ Signature

_____ Typed or printed name

PTO/SB/17 (11-00)
Approved for use through 10/31/2002. OMB 0651-0032

# FEE TRANSMITTAL FOR FY 2002

*Patent fees are subject to annual revision.*

**TOTAL AMOUNT OF PAYMENT** | $1,550.00

| *Complete if Known* | |
|---|---|
| Application Number | 09/578,895 |
| Filing Date | May 26, 2000 |
| First Named Inventor | Shunpei YAMAZAKI et al. |
| Examiner Name | G. Munson |
| Group Art Unit | 2811 |
| Attorney Docket No. | 740756-2160 |

## METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 19-2380 (740756-2160)

Deposit Account Name: Nixon Peabody LLP

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☒ **Payment Enclosed:**

☒ Check ☐ Credit Card ☐ Money Order ☐ Other

## FEE CALCULATION

### 1. BASIC FILING FEE

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 101 | 740 | 201 | 370 | Utility filing fee | |
| 106 | 330 | 206 | 165 | Design filing fee | |
| 107 | 510 | 207 | 255 | Plant filing fee | |
| 108 | 740 | 208 | 370 | Reissue filing fee | |
| 114 | 160 | 214 | 80 | Provisional filing fee | |

SUBTOTAL (1) $

### 2. EXTRA CLAIM FEES

| | | | Extra Claims | Fee from below | Fee Paid |
|---|---|---|---|---|---|
| Total Claims | | -20** = | | X | = |
| Independent Claims | | -3** = | | X | = |
| Multiple Dependent | | | | | = |

| Large Entity Fee Code | Large Entity Fee | Small Entity Fee Code | Small Entity Fee ($) | Fee Description |
|---|---|---|---|---|
| 103 | 18 | 203 | 9 | Claims in excess of 20 |
| 102 | 84 | 202 | 42 | Independent claims in excess of 3 |
| 104 | 280 | 204 | 140 | Multiple dependent claim, if not paid |
| 109 | 84 | 209 | 42 | ** Reissue independent claims over original patent |
| 110 | 18 | 210 | 9 | ** Reissue claims in excess of 20 and over original patent |

SUBTOTAL (2) $

**or number previously paid, if greater; For Reissues, see above

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 105 | 130 | 205 | 65 | Surcharge – late filing fee or oath | |
| 127 | 50 | 227 | 25 | Surcharge – late provisional filing fee or cover sheet | |
| 139 | 130 | 139 | 130 | Non-English transaction | |
| 147 | 2,520 | 147 | 2,520 | For filing a request for *ex parte* reexamination | |
| 112 | 920* | 112 | 920* | Requesting publication of SIR prior to Examiner action | |
| 113 | 1,840* | 113 | 1,840* | Requesting publication of SIR after Examiner action | |
| 115 | 110 | 215 | 55 | Extension for reply within first month | |
| 116 | 400 | 200 | 200 | Extension for reply **for the second and third months** | $810.00 |
| 117 | 920 | 460 | 460 | Extension for reply within third month | |
| 118 | 1,440 | 720 | 720 | Extension for reply within fourth month | |
| 128 | 1,960 | 228 | 980 | Extension for reply within fifth month | |
| 119 | 320 | 219 | 160 | Notice of Appeal | |
| 120 | 320 | 220 | 160 | Filing a brief in support of an appeal | |
| 121 | 280 | 221 | 140 | Request for oral hearing | |
| 138 | 1,510 | 138 | 1,510 | Petition to institute a public use proceeding | |
| 140 | 110 | 240 | 55 | Petition to revive – unavoidable | |
| 141 | 1,280 | 241 | 640 | Petition to revive – unintentional | |
| 142 | 1,280 | 242 | 640 | Utility issue fee (or reissue) | |
| 143 | 460 | 243 | 230 | Design issue fee | |
| 144 | 620 | 244 | 310 | Plant issue fee | |
| 122 | 130 | 122 | 130 | Petitions to the Commissioner | |
| 123 | 50 | 123 | 50 | Processing fee under 37 CR 1.17(q) | |
| 126 | 180 | 126 | 180 | Submission of Information Disclosure Stmt | |
| 581 | 40 | 581 | 40 | Recording each patent assignment per property (times number of properties) | |
| 146 | 740 | 246 | 370 | Filing a submission after final rejection (37 CFR § 1.129(a)) | |
| 149 | 740 | 249 | 370 | For each additional invention to be examined (37 CFR § 1.29(b)) | |
| 179 | 740 | 279 | 370 | Request for Continued Examination (RCE) | $740.00 |
| 169 | 900 | 169 | 900 | Request for expedited examination of a design application | |

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) $1,550.00

OIPE JC98 SEP 05 2003 TRADEMARK OFFICE

| SUBMITTED BY | | | | Complete *(if applicable)* | |
|---|---|---|---|---|---|
| Name *(Print/Type)* | Donald R. Studebaker | Registration No. *(Attorney/Agent)* | 32,815 | Telephone | (703) 770-9300 |
| Signature | | | | Date | July 29, 2002 |

NVA234747.1

# FEE TRANSMITTAL FOR FY 2003

*Patent fees are subject to annual revision.*

☐ Applicant claims small entity status. See 37 CFR 1.27

| TOTAL AMOUNT OF PAYMENT | ($)130.00 |
|---|---|

| *Complete if Known* | |
|---|---|
| Application Number | 09/578,895 |
| Filing Date | May 26, 2000 |
| First Named Inventor | Shunpei YAMAZAKI et al. |
| Examiner Name | Gene M. Munson |
| Art Unit | 2811 |
| Attorney Docket No. | 740756-2160 |

OT PTO SEP 05 2003 PATENT & TRADEMARK OFFICE

RECEIVED SEP 10 2003 OFFICE OF PETITIONS

## METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit Card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 19-2380 (740756-2160)

Deposit Account Name: Nixon Peabody LLP

**The Commissioner is authorized to:** *(check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

## FEE CALCULATION

### 1. BASIC FILING FEE

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 1001 | 750 | 2001 | 375 | Utility filing fee | |
| 1002 | 330 | 2002 | 165 | Design filing fee | |
| 1003 | 520 | 2003 | 260 | Plant filing fee | |
| 1004 | 750 | 2004 | 375 | Reissue filing fee | |
| 1005 | 160 | 2005 | 80 | Provisional filing fee | |

SUBTOTAL (1) ($) 0

### 2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

| | | Extra Claims | | Fee from below | | Fee Paid |
|---|---|---|---|---|---|---|
| Total Claims | -20** = | | X | | = | 0 |
| Independent Claims | -3** = | | X | | = | 0 |
| Multiple Dependent | | | X | | = | 0 |

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description |
|---|---|---|---|---|
| 1202 | 18 | 2202 | 9 | Claims in excess of 20 |
| 1201 | 84 | 2201 | 42 | Independent claims in excess of 3 |
| 1203 | 280 | 2203 | 140 | Multiple dependent claim, if not paid |
| 1204 | 84 | 2204 | 42 | ** Reissue independent claims over original patent |
| 1205 | 18 | 2205 | 9 | ** Reissue claims in excess of 20 and over original patent |

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | |
|---|---|---|---|---|---|
| 1051 | 130 | 2051 | 65 | Surcharge – late filing fee or oath | |
| 1052 | 50 | 2052 | 25 | Surcharge - late provisional filing fee or cover sheet | |
| 1053 | 130 | 1053 | 130 | Non-English specification | |
| 1812 | 2,520 | 1812 | 2,520 | For filing a request for *ex parte* reexamination | |
| 1804 | 920* | 1804 | 920* | Requesting publication of SIR prior to Examiner action | |
| 1805 | 1,840* | 1805 | 1,840* | Requesting publication of SIR after Examiner action | |
| 1251 | 110 | 2251 | 55 | Extension for reply within first month | |
| 1252 | 410 | 2252 | 205 | Extension for reply within second month | |
| 1253 | 930 | 2253 | 465 | Extension for reply within third month | |
| 1254 | 1,450 | 2254 | 725 | Extension for reply within fourth month | |
| 1255 | 1,970 | 2255 | 985 | Extension for reply within fifth month | |
| 1401 | 320 | 2401 | 160 | Notice of Appeal | |
| 1402 | 320 | 2402 | 160 | Filing a brief in support of an appeal | |
| 1403 | 280 | 2403 | 140 | Request for oral hearing | |
| 1451 | 1,510 | 1451 | 1,510 | Petition to institute a public use proceeding | |
| 1452 | 110 | 2452 | 55 | Petition to revive – unavoidable | |
| 1453 | 1,300 | 2453 | 650 | Petition to revive – unintentional | |
| 1501 | 1,300 | 2501 | 650 | Utility issue fee (or reissue) | |
| 1502 | 470 | 2502 | 235 | Design issue fee | |
| 1503 | 630 | 2503 | 315 | Plant issue fee | |
| 1460 | 130 | 1460 | 130 | Petitions to the Commissioner | 130.00 |
| 1807 | 50 | 1807 | 50 | Processing fee under 37 CFR 1.17(q) | |
| 1806 | 180 | 1806 | 180 | Submission of Information Disclosure Stmt | |
| 8021 | 40 | 8021 | 40 | Recording each patent assignment per property (times number of properties) | |
| 1809 | 750 | 2809 | 375 | Filing a submission after final rejection (37 CFR 1.129(a)) | |
| 1810 | 750 | 2810 | 375 | For each additional invention to be examined (37 CFR 1.129(b)) | |
| 1801 | 750 | 2801 | 375 | Request for Continued Examination (RCE) | |
| 1802 | 900 | 1802 | 900 | Request for expedited examination of a design application | |

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)130.00

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]

I hereby certify that this correspondence is being:

☐ deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop _____, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450

☐ transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (703) _____.

Date _____ Signature _____

Typed or printed name _____

## SUBMITTED BY

| Name *(Print/Type)* | Jeffrey L. Costellia | Registration No. *(Attorney/Agent)* | 35,483 | Complete *(if applicable)* Telephone | (202) 585-8000 |
|---|---|---|---|---|---|
| Signature | | | | Date | September 5, 2003 |

SEND TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

NVA276216.1

PATENT
740756-2160

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



| | | |
|---|---|---|
| In re Patent Application of: | ) | |
| Shunpei YAMAZAKI et al. | ) | Group Art Unit: 2811 |
| Serial No. 09/578,895 | ) | Examiner: Gene M. Munson |
| Filed: May 26, 2000 | ) | |
| For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC DEVICE | ) | Date: September 5, 2003 |

**PETITION, UNDER 37 C.F.R. 1.182, REQUESTING THE COMMISSIONER INVOKE SUPERVISORY AUTHORITY AND DIRECT THE EXAMINER TO CONSIDER THE INFORMATION DISCLOSURE STATEMENT FILED NOVEMBER 21, 2001 PURSUANT TO 37 C.F.R. 1.97 AND MPEP CHAPTER 609**

**MAIL STOP PETITION**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Petitioners request the Commissioner invoke supervisory authority to instruct Examiner Munson to fully consider each reference cited in the Information Disclosure Statement (IDS) filed November 30, 2001 (copy attached). Specifically, the petitioners request that the Examiner be instructed to consider each of the related U.S. Application Nos. 09/432,662 ('662), 09/580,485 ('485), 09/587,369 ('369), cited in the IDS of November 30, 2001, since that IDS filing was in complete compliance with the requirements of 37 C.F.R. 1.97 and 1.98.

The relevant facts concerning this request are as follows:

1. The instant application was filed on May 26, 2000.

2. A first Office Action was issued by Examiner Munson on July 30, 2001.

3. An Amendment and Information Disclosure Statement (IDS) were filed in response to the first Office Action on November 21, 2001 and November 30, 2001, respectively. The IDS included a PTO-1449 form listing the '662, '485 and '369 related applications and provided copies of the specification/drawings from each application.

4. A second final Office Action was issued by Examiner Munson on January 29, 2002 (copy attached) which included a copy of the PTO-1449 with the '662, '485 and '369 related application listings struck through and the notation "No copies nor indication that there are allowed pertinent claims to this invention" on the PTO-1449 form.

5. On February 27, 2002, the Applicants filed a Request For Acknowledgment Of Information Disclosure Statement which included a copy of the IDS and USPTO date stamped postcard for the IDS of November 30, 2001 and new copies of the '662, '485 and '369 related applications, as well as a further request to consider the related applications.

6. On June 6, 2002, the Applicants filed an Amendment which included, at page 4, another request to consider the '662, '485 and '369 related applications of the IDS of November 30, 2001 and outlined the reasons why the IDS must be considered by the Examiner, i.e., the IDS of November 30, 2001 was completely compliant with 37 C.F.R. §1.97-1.98.

7. On July 16, 2002, the Examiner issued an Advisory Action which included the notation at Box 11. "Contrary to response (p.4), there is nothing to consider for the patent applications, absent indication that there are allowed claims pertinent to this invention. No copy of indentified [sic] pending allowed claims has been provided, 37 C.F.R. 1.98. SN 09/432,662 will be considered if patent issues."

8. On July 29, 2002, the Applicants filed an RCE and a Preliminary Amendment (copy Attached) which included, at page 4, a renewed request for consideration of the '662, '485 and '369 related applications of the IDS of November 30, 2001 while pointing out the neither 37 C.F.R. 1.97 nor 1.98 contain any stipulation

that related U.S. patent applications must contain claims indicated as allowed, nor that copies of the allowed claims be provided before an Examiner will consider them.

9. On September 3, 2002, the Examiner issued an Office Action which included, at the paragraph bridging pages 3-4, the statement as follows:

"With regard to the remarks which accompany the preliminary amendment, filed 29 July 2002, no copy of pending claims for pending applications SN 09/432,662 has been provided. 37 C.F.R. 1.98. If provided, only allowed claims relevant to an existing claim in this application would be considered. 'There is no duty to submit information which is not material to the patentability of any existing claim.' 37 C.F.R. 1.56. Absent allowed claims in SN 09/432,662, there appears nothing to consider in SN 09/432,662 material to the patentability of any existing claim in this application. However, SN 09/432,662 will be considered if a patent issues." (Emphasis added)

10. On April 24 and 28, 2003, Mr. Massie of our office contacted Supervisory Patent Examiner (SPE) Mr. Thomas of TC Art Unit 2811 regarding a particular reason why the Examiner has not considered the '662, '485 and '369 related applications of the IDS of November 30, 2001 or provided an indication of such consideration by providing an initialed copy of the PTO-1449 form provided by the Applicants. After reviewing the file, SPE Thomas informed Mr. Massie that while he is sympathetic to the Applicants' request to consider the November 30th IDS, since Mr. Munson is a Primary Examiner he has little authority or influence in making the Examiner consider the '662, '485 and '369 related applications of the November 30th IDS. When asked if a Petition under 37 C.F.R. 1.181 would be an appropriate means to provide SPE Thomas with the authority to instruct the Examiner to consider the IDS, SPE Thomas informed Mr. Massie, that if filed, and placed before him for his decision he would **not grant such a petition**, but did not provide any further details as to the reason for such a denial except to say for the reasons of record advanced by Examiner Munson.

11. On May 2, 2003, the Applicants filed an RCE and Preliminary Amendment (copy attached) which included, at page 3, line 17, to page 4, line 6, a specific request "Should the Examiner maintain his position in this regard, he is again hereby

requested to provide support for such position by pointing out the specific text of 37 C.F.R. 1.98 requiring an indication that there are allowed claim pertinent to this invention set forth in the related applications."

12. On June 3, 2003, the Examiner issued a Notice of Allowability (PTOL-37 form) which included, at Box "Examiner's ~~Amendment~~/Comment - Re remarks (p 4-5) about IDS, see Office Action, dated 3 Sept. 2002, paper No. 17, pages 3-4, 37 CFR 1.56, 1.98."

13. On July 23, 2003, Mr. Massie of our office spoke on the telephone and then met briefly with Technology Director Arthur Grimley to outline Examiner Munson's refusal to consider what had been a proper and timely filed IDS on November 30, 2001. While Director Grimley had not had an opportunity to review the instant application file or to speak with the Examiner Munson and SPE Thomas, he understood the Applicants distress regarding having the IDS considered and was aware that Examiner Munson has been adamant in these situations. When the possibility of filing a petition in this matter, under 37 C.F.R. 1.182, was raised, Director Grimley acknowledged that such an alternative would appear to be appropriate in this instance.

14. On August 8, 2003, the Notice of Allowability was mailed in Application S.N. 09/580,485 (a copy of the allowed claims is attached)

15. On September 9, 2003, the Application S. N. 09/432,662 will issue as U.S. Patent No. 6,617,644 (a copy of the allowed claims is attached)

## Petitioners' Request

Since the Issue Fee is due for the instant application on September 3, 2003, it is imperative that the Petitioners receive consideration of this petition promptly in order to avoid the time and expense of having to file a Request to Withdraw from Issue under 37 C.F.R. 313 and RCE/CPA in order to avoid the patent from issuing without the '662, '485 and '369 related applications being considered and printed on the published patent. Further, the Petitioners respectfully request that the instant petition be granted and that the Examiner be instructed to consider the '662, '485 and '369 related applications filed with in the IDS of November 30, 2001. It is also requested that the Examiner be instructed to provide an indication of such consideration of the '662, '485 and '369 related applications by providing a completed References Cited (PTO-1449) form attached hereto along with a (Supplemental) Notice of Allowability (PTO-37) form as soon as possible in order that the patent can be issued with the listing of the '662, '485 and '369 related applications.

## Petitioners' Arguments

The Petitioners assert that throughout the prosecution of the present application Examiner Munson has failed to follow the requirements of MPEP Chapter 609 or understand the responsibilities of the Examiner under 37 C.F.R. 1.97.-1.98 or understand the responsibilities of the Petitioners and their representatives under 37 C.F.R. 1.56 which has resulted in the Examiner's improper decision to refuse consideration of the '662, '485 and '369 related applications.

Specifically, 37 C.F.R. 1.56 states:

> A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is

> cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by **§§ 1.97**(b)-(d) and **1.98**...
>
> Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and
>
> (1) It establishes, by itself or in combination with other information, a *prima facie* case of unpatentability of a claim; or
>
> (2) It refutes, or is inconsistent with, a position the applicant takes in:
>
> (i) Opposing an argument of unpatentability relied on by the Office, or
>
> (ii) Asserting an argument of patentability. (Emphasis added)

Therefore, § 1.56 places upon the Applicants and their representatives the responsibility of providing to the USPTO all information material to the patentability of at least one pending claim and that such material must be submitted during the examination period according the requirements of § 1.97 and § 1.98. According to § 1.56, it is the Applicants and their representatives who must determine the materiality under § 1.56 of any information and the Applicants or their representatives who must submit the material information, if known, to the USPTO for consideration.

The Applicants determined that submitted the originally filed '662, '485 and '369 related applications are material to the patentability of at least one claim of the instant application and as a result filed the Information Disclosure Statement of November 30, 2001 containing the '662, '485 and '369 related applications. The current version of 37 C.F.R. 1.97 requires:

> (a) In order for an applicant for a patent or for a reissue of a patent to have an information disclosure statement in compliance with § **1.98** considered by the Office during the pendency of the application, the information disclosure statement must satisfy one of paragraphs (b), (c), or (d) of this section...
>
> (c) An information disclosure statement shall be considered by the Office if filed after the period specified in paragraph (b) of this section, provided that

> the information disclosure statement is filed before the mailing date of any of a final action under § **1.113**, a notice of allowance under § **1.311**, or an action that otherwise closes prosecution in the application, and it is accompanied by one of:
>
> (1) The statement specified in paragraph (e) of this section; or
>
> (2) The fee set forth in § **1.17(p)**.

Therefore, since the November 30th IDS was filed before the final Office Action of January 29, 2002, the fee under § 1.17(p) was included. Additionally, § 1.98 requires that each IDS submitted include:

> (a) Any information disclosure statement filed under § **1.97** shall include:
>
> (1) A list of all patents, publications, applications, or other information submitted for consideration by the Office;
>
> (2) A legible copy of:...
>
> (iii) For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or that portion of the application which caused it to be listed including any claims directed to that portion; and...
>
> (3) Each U.S. application listed in an information disclosure statement must be identified by the inventor, application number, and filing date... (Emphasis added).

A further review of the November 30th IDS reveals that a legible copy of each of the originally filed '662, '485 and '369 related applications was included (each of which included the description, claims, abstract and drawings) and that the IDS listed each application by application number, filing date and inventor.

From the above facts it is clear that the Applicants fully complied with the requirements of § 1.56, § 1.97 and § 1.98 with regard to the '662, '485 and '369 related applications of the November 30th IDS.

MPEP Chapter 609 outlines the requirements of § 1.56, § 1.97 and § 1.98 and sets forth the responsibilities of the USPTO once a proper IDS submission is made by stating:

> ...An information disclosure statement **filed in accordance with the provisions of 37 CFR 1.97 and 37 CFR 1.98 will be considered by the examiner assigned to the application.** The requirements for the content of a statement have been simplified in the rules, to encourage individuals

> associated in a substantive way with the filing and prosecution of a patent application to submit information to the Office so the examiner can evaluate its relevance to the claimed invention. The procedures for submitting an information disclosure statement under the rules are designed to encourage individuals to submit information to the Office promptly and in a uniform manner. These rules provide certainty for the public by defining the requirements for submitting information disclosure statements to the Office so that the Office will consider information contained therein before a patent is granted... (Emphasis added)

Further, MPEP Chapter 609 (III)(A) sets for the minimum requirements for an information disclosure statement by stating:

> ...Each information disclosure statement must include a list of all patents, publications, U.S. applications, or other information submitted for consideration by the Office.
>
> 37 CFR 1.98(b) requires that each item of information in an IDS be identified properly. U.S. patents must be identified by the inventor, patent number, and issue date. U.S. patent application publications must be identified by the applicant, patent application publication number, and publication date. U.S. applications must be identified by the inventor, the eight digit application number (the two digit series code and the six digit serial number), and the filing date...
>
> The list of information complying with the identification requirements of 37 CFR 1.98(b) may not be incorporated into the specification of the application in which it is being supplied, but must be submitted in a separate paper....Use of either form PTO-1449, Information Disclosure Citation, or PTO/SB/08A and 08B, Information Disclosure Statement, to list the documents is encouraged. See subsection C(2) below.
>
> A (2) Legible Copies
>
> In addition to the list of information, each information disclosure statement must also include a legible copy of:...
>
> (C) For each cited pending U.S. application, the application specification including the claims, and any drawings of the application, or that portion of the application which caused it to be listed including any claims directed to that portion

Therefore, from the review of the November 30th IDS above, it is clearly evident that the submission of the '662, '485 and '369 related applications was in complete compliance with § 1.97 and § 1.98 and, therefore, the '662, '485 and '369

related applications must be considered by the Examiner during the examination of the instant application.

With regard to the Examiner's stated reasons for not considering the '662, '485 and '369 related applications of the November 30th IDS, neither § 1.97, § 1.98 or MPEP Chapter 609 set forth any requirement that, in order to have related patent applications be considered by the Examiner, the Applicants must provide an:

a. "indication that there are allowed pertinent claims to this invention" or

b. "...absent indication that there are allowed claims pertinent to this invention. No copy of indentified [sic] pending allowed claims has been provided, 37 C.F.R. 1.98. SN 09/432,662 will be considered if patent issues" or

c. "...no copy of pending claims for pending applications SN 09/432,662 has been provided. 37 C.F.R. 1.98"

Further, the Examiner has steadfastly refused to provide any elaboration or legal precedence to support the alleged requirements for filing consideration of the related applications in an IDS. Finally, it is noted that the Examiner has stated, in the Office Action of September 3, 2002 (see paragraph bridging pages 3-4) that "**there appears nothing to consider in SN 09/432,662 material to the patentability of any existing claim in this application.**" Such a statement is an admission that the Examiner has in fact considered the '662 application. Accordingly, the Examiner should have indicated such consideration on a References Cited ( PTO-892) form to accompany the September 3, 2002 Office Action.

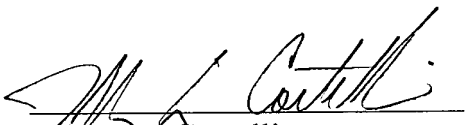
In view of the arguments and evidence provided, the Petitioners respectfully request that the instant petition be granted and that the Examiner be instructed to consider the '662, '485 and '369 related applications filed with in the IDS of November 30, 2001. It is also requested that the Examiner be instructed to provide an indication of such consideration of the '662, '485 and '369 related applications by providing a completed References Cited (PTO-1449) form attached hereto along with a (Supplemental) Notice of Allowability (PTO-37) form as soon as possible.

This petition is submitted under 37 C.F.R. 1.182 since SPE Thomas has effectively denied a petition under 37 C.F.R. 1.181 during his discussion with Mr.

Massie on April 28, 2003. However, should the Commissioner regard the filing of the instant petition under § 1.182 as inappropriate, then it is respectfully requested that the Commissioner accept this petition as having been made under 37 C.F.R. 1.181 (no fee). A check for the petition fee, under 37 C.F.R. 1.17(h), is enclosed, however, should the check become lost or misplaced the Commissioner is hereby authorized to charge the required fee ($130.00), under 37 C.F.R. 1.17(h), to Deposit Account No. 19-2380 (740756-2160).

Prompt attention to this matter is appreciated.

Respectfully submitted,



Jeffrey L. Costellia
Registration No. 35,483

NIXON PEABODY LLP
Suite 900
401 9th Street, N.W.
Washington D.C. 20004
(202) 585-8000
(202) 585-8080 fax

**Attachments**:
Copy of PTO-1449 listing U.S. Application Nos. 09/432,662, 09/580,485, 09/587,369
Copy of IDS of November 30, 2001
Copy of Office Action of January 29, 2002
Copy of RCE/Preliminary Amendment of July 29, 2002
Copy of RCE/Preliminary Amendment of May 2, 2003
Copy of allowed claims in Application S.N. 09/580,485
Copy of allowed claims in Application S.N. 09/432,662

| Form PTO-1449 (Rev. 8-83) | U.S. Department of Commerce Patent and Trademark Office | Atty Docket 0756-2160 | Serial No. 09/578,895 |
|---|---|---|---|
| **INFORMATION DISCLOSURE STATEMENT** | | Applicants: Shunpei YAMAZAKI et al. | |
| | | Filing Date: May 26, 2000 | Group Art Unit: 2775 |

**U.S. PATENT DOCUMENTS**

| Examiner Initial | Document Number | Date | Name | Class | Subclass | Filing Dat (if appropriate) |
|---|---|---|---|---|---|---|
| | | | | | | |
| | | | | | | |



**OTHER DOCUMENT** (Including Author, Title, Date, Pertinent Pages, Etc.)

| Examiner Initial | |
|---|---|
| | Specification & Drawings of US Patent Application No. 09/432,662 |
| | Specification & Drawings of US Patent Application No. 09/580,485 |
| | Specification & Drawings of US Patent Application No. 09/587,369 |



| Examiner | Date Considered |
|---|---|

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this formwith next communication to applicant.

This will acknowledge receipt of the following:

1. Information Disclosure Statement and Notification of Related Application w/ Certificate of Mailing
2. Form PTO-1449 (with 5 references)



in re PATENT application of:

Shunpei YAMAZAKI et al.

Serial No. 09/578,895

Filed: May 26, 2000

Title: ELECTRO-OPTICAL DEVICE AND ELECTRONIC DEVICE

Due date: 10/30/2001



Nov. 30, 2001

Docket No. 740756-2160
JLC/mlc

Letter: 10/26/2001

Hand-Carry



Pam

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of: )
Shunpei YAMAZAKI et al. ) Art Unit: 2811
Serial No. 09/578,895 ) Examiner: G. Munson
Filed: May 26, 2000 )
For: ELECTRO-OPTICAL DEVICE )
AND ELECTRONIC DEVICE ) Hand Carry November 30, 2001





**INFORMATION DISCLOSURE STATEMENT AND NOTIFICATION OF RELATED APPLICATION**

Commissioner for Patents and Trademarks
Washington, D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, it is requested that the reference(s) listed on the attached Form PTO-1449 be made of record in the above-identified application.

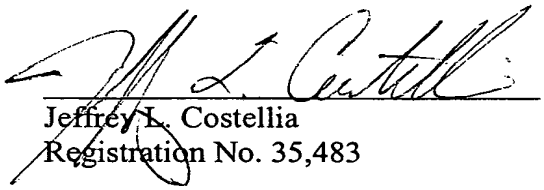
U.S. Patent Nos. 5,729,308 and 6,236,064 may disclose the use of a multi-gate TFT and an electroluminescence device. The subject invention can be distinguished from these references because they do not disclose a connection of two thin film transistors claimed in the present invention. Copies of the references are submitted herewith in accordance with 37 C.F.R. 1.98(a).

Further, pursuant to Applicant's duty of candor under 37 C.F.R. §1.56, Applicants wish to inform the Examiner of the following applications claiming related subject matter and hereby submit copies of the following applications for the Examiner's consideration:

| SERIAL NO. | FILING DATE | INVENTORS |
|---|---|---|
| 09/432,662 | November 3, 1999 | Yamazaki et al. |
| 09/580,485 | May 30, 2000 | Yamazaki et al. |
| 09/587,369 | June 2, 2000 | Yamazaki et al. |

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 19-2380 (740756-2160).

Respectfully submitted,



Jeffrey L. Costellia
Registration No. 35,483

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

| Form PTO-1449 (Rev. 8-83) | U.S.Department of Commerce Patent and Trademark Office | Atty Docket 0756-2160 | Serial No. 09/578,895 |
|---|---|---|---|
| INFORMATION DISCLOSURE STATEMENT | | Applicants: Shunpei YAMAZAKI et al. | |
| | | Filing Date: May 26, 2000 | Group Art Unit: 2775 |

**U.S. PATENT DOCUMENTS**

| Examiner Initial | Document Number | Date | Name | Class | Subclass | Filing Date (if appropriate) |
|---|---|---|---|---|---|---|
| | 5,729,308 | 03/17/1998 | Yamazaki et al. | | | |
| | 6,236,064 | 05/22/2001 | Mase et al. | | | |

**OTHER DOCUMENT** (Including Author, Title, Date, Pertinent Pages, Etc.)

| Examiner Initial | |
|---|---|
| | Specification & Drawings of US Patent Application No. 09/432,662 |
| | Specification & Drawings of US Patent Application No. 09/580,485 |
| | Specification & Drawings of US Patent Application No. 09/587,369 |



| Examiner | Date Considered |
|---|---|

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this formwith next communication to applicant.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/578,895 | 05/26/2000 | Shunpei Yamazaki | 0756-2160 | 8423 |

22204 7590 01/29/2002

NIXON PEABODY, LLP
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN, VA 22102

| EXAMINER |
|---|
| MUNSON, GENE M |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 01/29/2002



Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

| Application No. | Applicant(s) |
|---|---|
| 578,895 | S. YAMAZAKI ET AL |
| **Examiner** | **Group Art Unit** |
| G. MUNSON | 2811 |



*—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE THREE MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).



**Status**

☒ Responsive to communication(s) filed on 21 NOVEMBER 2001

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

**Disposition of Claims**

☒ Claim(s) 1-10, 14-51 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☒ Claim(s) 3, 4, 7, 10, 29-31, 33-36, 38, 39, 41, 42, 44-47, 49, 50 is/are allowed.

☒ Claim(s) 1, 2, 5, 6, 14-18, 20, 23-28, 32, 37, 40, 43, 48, 51 is/are rejected.

☒ Claim(s) 8, 9, 19, 21, 22 is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

**Application Papers**

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119 (a)-(d)**

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

**Attachment(s)**

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 5

☐ Interview Summary, PTO-413

☐ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

**Office Action Summary**

Claims 14-16, 24, 28, 32, 37, 40, 43, 48 and 51 are rejected under 35 U.S.C. 112, second and fourth paragraphs. It is unclear how the claims further limit the electroluminescence display device of claims 1-3, 17, 25, 29, 33, 38, 41, 44 and 49. This rejection could be overcome if each of the claims were put in independent form including the limitations of the claims on which they depend.

Claims 14-16, 24, 28, 32, 37, 40, 43, 48 and 51 are rejected under 35 U.S.C. 112, first paragraph. The listed "electronic" devices are not clearly described to enable a person skilled in the art to make and use the devices. Figures 16 and 20 may be sufficient for a design patent but not for a utility patent.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 5, 6, 17, 18, 20, 23 and 25-27 are rejected under 35 U.S.C. 102 as unpatentable as shown by Tang et al '365 *of record*. The "channel" and "impurity" regions read on inherent subportions of a channel in TFT1 of Tang et al (Figure 2).

Claims 1, 2, 5, 6, 17, 18, 20, 23 and 25-27 are rejected under 35 U.S.C. 102 as unpatentable as shown by Hosokawa Japanese document 10-189252 *of record*. The "channel" and "impurity" regions read on inherent subportions of a channel in transistor 21 of Hosokawa (Figures 2, 3).

Claims 14-16, 24 and 28 are rejected under 35 U.S.C. 103 as unpatentable over Tang et al '365 and Hosokawa Japan document 10-189252, considered together. It would have been obvious to use pixels as in Tang et al (Figure 2) and Hosokawa (Figures 2, 3) in order to achieve flat panel displays for known electronic devices as claimed.

The arguments in the response, filed 21 November 2001, have been considered but are not wholly persuasive. Contrary to the response (pages 14-15), the rejected claims are not limited to a "multi-gate structure".

Claims 3, 4, 7, 10, 29-31, 33-36, 38, 39, 41, 42, 44-47, 47, 49 and 50 are allowed. Moreover, claims 8, 9, 19, 21 and 22 are objected to as dependent upon rejected claims but would be allowable if claims 8, 9, 19 and 21 were each put in completed form as independent claims including all limitations of claims 1, 8; 2, 9; 17, 19; 17, 21.

This action is **FINAL**.

This action is a **final rejection** and is intended to close the prosecution of this application. Applicant's reply under 37 CFR 1.113 to this action is limited either to an appeal to the Board of Patent Appeals and Interferences or to an amendment complying with the requirements set forth below.

If applicant should desire to appeal any rejection made by the examiner, a Notice of Appeal must be filed within the period for reply identifying the rejected claim or claims appealed. The Notice of Appeal must be accompanied by the required appeal fee of appropriate amount.

If applicant should desire to file an amendment, entry of a proposed amendment after final rejection cannot be made as a matter of right unless it merely cancels claims or complies with a formal requirement made earlier. Amendments touching the merits of the application which otherwise might not be proper may be admitted upon a showing a good and sufficient reasons why they are necessary and why they were not presented earlier.

A reply under 37 CFR 1.113 to a final rejection must include the appeal from, or cancellation of, each rejected claim. The filing , whichever is longer, of an amendment after final rejection, whether or not it is entered, does not stop the running of the statutory period for reply to the final

rejection unless the examiner holds the claims to be in condition for allowance. Accordingly, if a Notice of Appeal has not been filed properly within the period for reply, or any extension of this period obtained under either 37 CFR 1.136(a) or (b), the application will become abandoned.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to G. Munson at telephone number (703) 308-4925 or 0956.

Munson/nt

1-23-02

GENE M. MUNSON
EXAMINER
GROUP ART UNIT 2811

#5



Form PTO-1449 (Rev. 8-83) | U.S. Department of Commerce Patent and Trademark Office

**INFORMATION DISCLOSURE STATEMENT**

| | |
|---|---|
| **Atty Docket** 0756-2160 | **Serial No.** 09/578,895 |
| **Applicants:** Shunpei YAMAZAKI et al. | |
| **Filing Date:** May 26, 2000 | **Group Art Unit:** ~~2775~~ 2871 |



**U.S. PATENT DOCUMENTS**

| Examiner Initial | Document Number | Date | Name | Class | Subclass | Filing Date (if appropriate) |
|---|---|---|---|---|---|---|
| GMK | 5,729,308 | 03/17/1998 | Yamazaki et al. | — | — | |
| GMK | 6,236,064 | 05/22/2001 | Mase et al. | — | — | |



**OTHER DOCUMENT** (Including Author, Title, Date, Pertinent Pages, Etc.)

| Examiner Initial | |
|---|---|
| | ~~Specification & Drawings of US Patent Application No. 09/432,662~~ |
| | ~~Specification & Drawings of US Patent Application No. 09/580,485~~ |
| | ~~Specification & Drawings of US Patent Application No. 09/587,369~~ |

No copies nor indication that there are allowed pertinent claims to this invention.



| | |
|---|---|
| Examiner G. MUNSON | Date Considered 18 JANUARY 2002 |

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this formwith next communication to applicant.

Receipt is acknowledged on: July 29, 2002

In re the **Request for Continued Examination (RCE)** of: Shunpei YAMAZAKI et al.
Serial No. 09/578,895 Filed: May 26, 2000
For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC DEVICE

Petition for Extension of Time (duplicate)
Request for Continued Examination (RCE) Transmittal and Fee Transmittal (duplicate)
Preliminary Amendment
Check No. 5288 in the amount of $1,550.00
($740 RCE Fee, $810 Extension Fee)

DRS/JLC/rmg
(740756-2160)

**HANDCARRY**

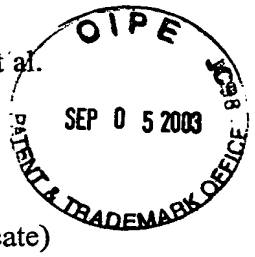
Due Date: 07/29/2002





8/7/02

Receipt is acknowledged on: July 29, 2002




In re the **Request for Continued Examination (RCE)** of: Shunpei YAMAZAKI et al.
Serial No. 09/578,895 Filed: May 26, 2000
For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC DEVICE

Petition for Extension of Time (duplicate)
Request for Continued Examination (RCE) Transmittal and Fee Transmittal (duplicate)
Preliminary Amendment
Check No. 5288 in the amount of $1,550.00
($740 RCE Fee, $810 Extension Fee)

DRS/JLC/rmg
(740756-2160)

**HANDCARRY**

Due Date: 07/29/2002

THIS DOCUMENT HAS VISIBLE AND INVISIBLE FLUORESCENT FIBERS - VIEW UNDER BLACK LIGHT - TRUE WATERMARK IN PAPER - HOLD TO LIGHT TO VIEW

7/29/02

NIXON PEABODY LLP
ATTORNEYS AT LAW

PATENT DISBURSEMENT ACCOUNT
8180 Greensboro Drive
Suite 800
McLean, VA 22102

CHASE MANHATTAN BANK, N.A.
ROCHESTER, NY

5288

50-17
223

PAY THE SUM 1550 DOLLARS AND 00 CENTS********** $ 1550.00*

PAY EXACTLY

TO THE ORDER OF COMMISSIONER FOR PATENTS AND TRADEMARKS

Linda Rutter MP

740756-2160

Vendor # 740101
Request # 439425

DOCUMENT CONTAINS VOID PANTOGRAPH AND MICRO-PRINT SIGNATURE LINE - MAGNIFY TO VIEW

⑈005288⑈ ⑆022300173⑆ 51206045 2⑈

PTO/SB/22 (10-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE


# PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number: 740756-2160

In re Application of: Shunpei YAMAZAKI et al.

Application Number: 09/578,895 | Filed: May 26, 2000

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC DEVICE

Group Art Unit: 2811 | Examiner: G. Munson



This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and appropriate non-small-entity fee are as follows (check time period desired):

- ☐ One month (37 CFR 1.17(a)(1)) - ($55/$110) $_____
- ☒ Second and Third Months (37 CFR 1.17(a)(2)) $810.00
  First month previously paid May 29, 2002
- ☐ Three month (37 CFR 1.17(a)(3)) - ($460/$920) $_____
- ☐ Four month (37 CFR 1.17(a)(4)) - ($720/$1440) $_____
- ☐ Five month (37 CFR 1.17(a)(5)) - ($980/$1960) $_____

☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee amount shown above is reduced by one-half, and the resulting fee is $_____

☒ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Commissioner has already been authorized to charge fees in this application to a Deposit Account.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 19-2380.
I have enclosed a duplicate copy of this sheet.

I am the ☐ applicant/inventor

☐ assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ attorney or agent of record.

☐ attorney or agent under 37 CFR 1.34(a).
Registration number if acting under 37 CFR 1.34(a) _____

**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**

July 29, 2002
Date


Signature

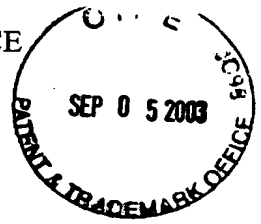
Donald R. Studebaker
Typed or printed name

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☐ Total of _____ forms are submitted.


NVA234744.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE




| | | |
|---|---|---|
| In re Patent Application of | ) | |
| Shunpei YAMAZAKI et al. | ) | |
| Serial No. 09/578,895 | ) | Art Unit: 2811 |
| Filed: May 26, 2000 | ) | Examiner: G. Munson |
| For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC DEVICE | ) | Date: July 29, 2002 |

PRELIMINARY AMENDMENT

Honorable Commissioner for Patents and Trademarks
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE CLAIMS:

Please amend claims 1, 2, 17 and 25 as follows: Please note that the claims are presented below in their amended form. They are further presented as an Attachment to the Amendment whereby the amendments to the claims are outlined using the conventional method of bracketing and underlining.

1. (Twice Amended) An electroluminescence display device comprising:
a substrate;

a plurality of pixels over the substrate, each of the plurality of pixels comprising:

a first thin film transistor;

a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor; and

an electroluminescence element electrically connected to the second thin film transistor,

wherein the first thin film transistor comprises at least two channel regions in an active layer, at least two gate electrodes corresponding to the channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions.

2. (Twice Amended) An electroluminescence display device comprising:

a substrate; and

a plurality of pixels over the substrate, each of the plurality of pixels comprising:

a first thin film transistor;

a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor; and

an electroluminescence element electrically connected to the second thin film transistor,

wherein the first thin film transistor comprises at least two channel regions in an active layer, at least two gate electrodes corresponding to the channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions, and

wherein a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor.

17. (Amended) An electroluminescence display device comprising:

a substrate; and

a plurality of pixels over the substrate, each of the plurality of pixels comprising:

a first thin film transistor;

a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor; and

an electroluminescence element electrically connected to the second thin film transistor,

wherein the first thin film transistor comprises at least two gate electrodes over the substrate, at least two channel regions corresponding to the gate electrode, over the gate electrode with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions.

25. (Amended) An electroluminescence display device comprising:

a substrate; and

a plurality of pixels over the substrate, each of the plurality of pixels comprising:

a first thin film transistor;

a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor; and

an electroluminescence element electrically connected to the second thin film transistor,

wherein the first thin film transistor comprises at least two gate electrodes over the substrate, at least two channel regions corresponding to the gate electrode, over the gate electrode with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions, and

wherein a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor.

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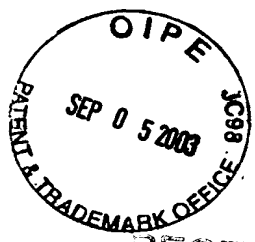




This will acknowledge receipt of the following:
1. REQUEST FOR CONTINUED EXAMINATION (RCE)
2. PETITION FOR EXTENSION OF TIME (ONE MONTH)
3. PRELIMINARY AMENDMENT
4. CHECK No. 7730, $860.00 ($750-RCE; $110-EXT)

In re Patent Application of:
Inventors: Shunpei YAMAZAKI et al.
Serial No.: 09/578,895
Filed: May 26, 2000
Title: ELECTRO-OPTICAL DEVICE AND ELECTRONIC DEVICE

**Due Date: April 27, 2003**
**Docket No. 740756-2160**

DRS/LCD/dam
Date: 4/28/2003

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ATTORNEYS AT LAW

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Suite 800
McLean, VA 22102

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# REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

**Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995. See The American Inventors Protection Act of 1999 (AIPA).**

| | |
|---|---|
| Application Number | 09/578,895 |
| Filing Date | May 26, 2000 |
| First Named Inventor | Shunpei YAMAZAKI et al |
| Group Art Unit | 2811 |
| Examiner Name | Gene M. Munson |
| Attorney Docket Number | 740756-2160 |



This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.

NOTE: 37 C.F.R. § 1.114 is effective on May 29, 2000. If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. § 1.53(d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Final Rule, 65 Fed. Reg. 50092 (Aug. 16, 2000); Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 Off. Gaz. Pat. Office 47 (Apr. 11, 2000), which established RCE practice.



1. Submission required under 37 C.F.R. § 1.114
   - a. ☐ Previously submitted
     - i. ☐ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on _____ (Any unentered amendment(s) referred to above will be entered).
     - ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - iii. ☐ Other _____
   - b. ☒ Enclosed
     - i. ☐ Amendment/Reply
     - ii. ☐ Affidavit(s)/Declaration(s)
     - iii. ☐ Information Disclosure Statement (IDS)
     - iv. ☒ Other PRELIMINARY AMENDMENT
2. Miscellaneous
   - a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. § 1.17(i) required)
   - b. ☐ Other _____
3. Fees — The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.
   - a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 19-2380
     - i. ☒ RCE fee required under 37 C.F.R. § 1.17(e)
     - ii. ☒ Extension of time fee (37 C.F.R. §§ 1.136 and 1.17)
     - iii. ☐ Other _____
   - b. ☒ Check in the amount of $860.00 enclosed
   - c. ☐ Payment by credit card (Form PTO-2038 enclosed)

**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED**

| | | | |
|---|---|---|---|
| Name (Print/Type) | Luan C. Do | Registration No. (Attorney/Agent) | 38,434 |
| Signature | | Date | April 28, 2003 |

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| Name (Print/Type) | Deborah Movahhedi | | |
| Signature | Deborah Movahhedi | Date | April 28, 2003 |

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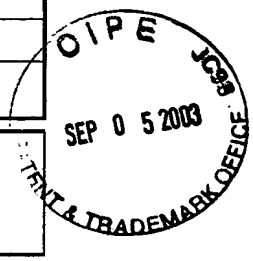
# REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

**Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995. See The American Inventors Protection Act of 1999 (AIPA).**

| | |
|---|---|
| Application Number | 09/578,895 |
| Filing Date | May 26, 2000 |
| First Named Inventor | Shunpei YAMAZAKI et al. |
| Group Art Unit | 2811 |
| Examiner Name | G. Munson |
| Attorney Docket Number | 740756-2160 |

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NOTE: 37 C.F.R. § 1.114 is effective on May 29, 2000. If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. § 1.53(d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Final Rule, 65 Fed. Reg. 50092 (Aug. 16, 2000); Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 Off. Gaz. Pat. Office 47 (Apr. 11, 2000), which established RCE practice.

1. Submission required under 37 C.F.R. § 1.114
   - a. ☒ Previously submitted
     - i. ☒ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on May 29, 2002 (Any unentered amendment(s) referred to above will be entered).
     - ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - iii. ☐ Other _____
   - b. ☒ Enclosed
     - i. ☒ Preliminary Amendment
     - ii. ☐ Affidavit(s)/Declaration(s)
     - iii. ☐ Information Disclosure Statement (IDS)
     - iv. ☒ Petition for Extension of Time
2. Miscellaneous
   - a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. § 1.17(I) required)
   - b. ☐ Other _____
3. Fees — The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.
   - a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No.19-2380.
     - i. ☒ RCE fee required under 37 C.F.R. § 1.17(e)
     - ii. ☒ Extension of time fee (37 C.F.R. §§ 1.136 and 1.17)
     - iii. ☐ Other _____
   - b. ☒ Check in the amount of $1,550.00 enclosed
   - c. ☐ Payment by credit card (Form PTO-2038 enclosed)

**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED**

| | | | |
|---|---|---|---|
| Name *(Print/Type)* | Donald R. Studebaker | Registration No. *(Attorney/Agent)* | 32,815 |
| Signature | | Date | July 29, 2002 |

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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| PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) | Docket Number (Optional) 740756-2160 |
|---|---|

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Deborah Movahhedi
Name: DEBORAH MOVAHHEDI

| | |
|---|---|
| In re Application of Shunpei YAMAZAKI et al. | |
| Application Number 09/578,895 | Filed May 26, 2000 |
| For ELECTRO-OPTICAL DEVICE AND ELECTRONIC DEVICE | |
| Group Art Unit 2811 | Examiner Gene M. Munson |

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This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and appropriate non-small-entity fee are as follows (check time period desired):

- ☒ One month (37 CFR 1.17(a)(1)) - ($55/$110) $110.00
- ☐ Two months (37 CFR 1.17(a)(2)) - ($205/$410) $_____
- ☐ Three months (37 CFR 1.17(a)(3)) - ($465/$930) $_____
- ☐ Four months (37 CFR 1.17(a)(4)) - ($725/$1450) $_____
- ☐ Five months (37 CFR 1.17(a)(5)) - ($985/$1970) $_____

☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee amount shown above is reduced by one-half, and the resulting fee is $_____.

☒ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Commissioner has already been authorized to charge fees in this application to a Deposit Account.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 19-2380. I have enclosed a duplicate copy of this sheet.

I am the ☐ applicant/inventor

☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ attorney or agent of record.

☐ attorney or agent under 37 CFR 1.34(a). Registration number if acting under 37 CFR 1.34(a) _____.

**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**

April 28, 2003
Date

Signature

Luan C. Do, Reg. No. 38,434
Typed or printed name

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☐ Total of _____ forms are submitted.

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NVA262884.1

Docket No. 740756-2160

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE


| | | |
|---|---|---|
| In re Patent Application of: | ) | |
| Shunpei YAMAZAKI et al. | ) | Group Art Unit: 2811 |
| Serial No. 09/578,895 | ) | Examiner: Gene M. Munson |
| Filed: May 26, 2000 | ) | |
| For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC DEVICE | ) | Date: April 28, 2003 |



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Deborah Movahhedi

Deborah Movahhedi

**PRELIMINARY AMENDMENT**

Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the final Office Action mailed December 27, 2002, please consider the following Request for Continued Examination (RCE), amendments and remarks in connection with the above-identified application.

IN THE SPECIFICATION:

**Page 56, first full paragraph, please replace with the following:**

In embodiment 11, examples of the pixel structure of the EL display device of the present invention are shown in Figs. 21A and 21B. Note that in embodiment 11, reference numeral 4701 denotes a source wiring of a switching TFT 4702, reference numeral 4703 denotes a gate wiring of the switching TFT 4702, reference numeral 4704 denotes a current control TFT, 4705 denotes an electric current supply line, 4706 denotes a power source control TFT, 4707 denotes a power source control gate wiring, and 4708 denotes an EL element. Japanese Patent Application ~~Laid-open~~ No. Hei 11-341272 may be referred to regarding the operation of the power source control TFT 4706.

IN THE CLAIMS:

Please cancel claims 14-16, 24, 28, 32, 37, 40, 43, 48, 51 and 54 without prejudice or disclaimer of the subject matter recited therein.

## REMARKS

The Examiner's final Office Action of December 27, 2002 has been received and its contents reviewed. Applicants' would like to thank the Examiner for the consideration given to the above-identified application, and for indicating the allowance of claims 2-4, 6, 7, 9, 10, 25-27, 29-31, 38, 39, 41, 42, 49, 50, 52 and 53. Further, the Examiner is thanked for indicating in the telephonic conference on April 28, 2003 that the review of this Preliminary Amendment will be sufficiently delayed until copies of a small number of references to be submitted in an IDS are available and submitted, as per Applicants' request.

By the above actions, claims 14-16, 24, 28, 32, 37, 40, 43, 48, 51 and 54 have been cancelled. Accordingly, claims 1-10, and 17-23, 25-27, 29-31, 33-36, 38-39, 41, 42, 44-47, 49-50, and 52-53 are pending for consideration, of which claims 1-3, 17, 25, 29, 33, 38, 41, 44, 49 and 52 are independent. In view of these actions and the following remarks, reconsideration of this application is now requested.

Before turning to the detailed Office Action, Applicants again would like to request the Examiner to consider the related application Serial No. 09/432,662 submitted in the IDS of November 30, 2001 for the reason as follows:

The Examiner has indicated in the Advisory Action mailed July 16, 2002, for example, that no copy of identified pending allowed claims has been provided in accordance with 37 C.F.R. 1.98, and that SN 09/432,662 will be considered if a patent issues. It is unclear why the Examiner believes that there is any requirement that patent applications disclosed to the U.S. Patent and Trademark Office under applicants' duty of disclosure set forth in 37 C.F.R. 1.56 which are filed in compliance with 37 C.F.R. 1.98 require an indication that there are allowed claims pertinent to this invention set forth in the related applications.

Further, as previously submitted, while such allowed claims may be relevant to the issue of double patenting, there is no such requirement for the Examiner to indicate consideration of the subject matter set forth in the related applications. Accordingly, in that the U.S. Patent and Trademark Office has placed this burden on the applicant, it is only fitting that the Examiner indicate his consideration of the related applications submitted in accordance therewith. Such

applications include U.S. Application Serial Nos. 09/432,662; 09/580,485 and 09/587,369 as identified in applicants' Form PTO-1449 filed November 30, 2001.

Should the Examiner maintain his position in this regard, he is again hereby requested to provide support for such position by pointing out the specific text of 37 C.F.R 1.98 requiring an indication that there are allowed claims pertinent to this invention set forth in the related applications.

Referring now to the detailed Office Action, claims 14-16, 24, 28, 32, 37, 40, 43, 48, 51 and 54 are rejected under 35 U.S.C. §112, first, second and fourth paragraphs. In response, and in order to expedite the prosecution of this application, Applicants have canceled claims 14-16, 24, 28, 32, 37, 40, 43, 48, 51 and 54 as shown above, without prejudice to file a divisional application directed thereto. Accordingly, Applicants respectfully request reconsideration and withdrawal of the §112, first, second and fourth paragraphs, rejections.

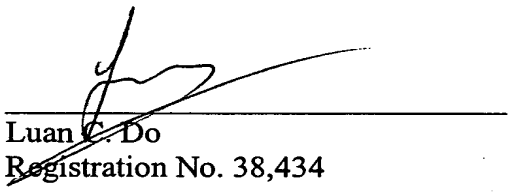
Claims 1, 5, 17, 20, 23, 33, 36, 44 and 47 stand rejected under 35 U.S.C. §102(b) as unpatentable over Yamada. Further, claims 14, 24, 37 and 48 stand rejected 35 U.S.C. §103(a) as unpatentable over Yamada and Tang et al. (U.S. Patent No. 5,684,365 of record – hereafter Tang), and claims 8, 18, 19, 21, 22, 34, 35, 45 and 45 stand objected to as dependent upon rejected claims but would be allowable if these claims are rewritten as independent claims including all limitations of a base claim and any intervening claims.

In response to the rejections, Applicants have submitted on December 31, 2002 a verified English translation of priority document Japanese Patent Application Serial No. 11-158787, which was filed on June 4, 1999 prior to effective U.S. filing date of the Yamada reference, which is November 30, 1999. Therefore, Applicants have perfected the claimed priority date, and the Yamada reference does not qualify as prior art.

In view of the amendments and arguments set forth above, Applicants respectfully request reconsideration and withdrawal of the pending §102(b) over Yamada and the pending §103(a) rejection over Yamada in view of Tang, as well as the objection to claims 8, 18, 19, 21, 22, 34, 35, 45 and 45.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise which could be eliminated through discussion with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,



Luan C. Do
Registration No. 38,434

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, VA 22102
(703) 770-9300

Allowed Claims for Serial No. 09/580,485
Your Reference: US4213
Our Reference: 740756-2154

CLAIMS AS ALLOWED

1. A method for manufacturing an electrical device, said method comprising:

forming at least a thin film transistor on an insulating surface;

forming a first insulating film comprising an organic resin over the thin film transistor;

forming a second insulating film comprising silicon nitride on the first insulating film;

forming a pixel electrode on the second insulating film, said pixel electrode electrically connected to the thin film transistor;

forming an EL layer over the pixel electrode;

forming a second electrode over the EL layer,

wherein the EL layer is selectively formed through an ink jet method.

2. A method for manufacturing an electrical device, said method comprising:

forming at least a thin film transistor;

forming a first insulating film comprising an organic resin over the thin film transistor;

forming a second insulating film comprising at least one selected from the group consisting of aluminum oxide, aluminum nitride and nitrated aluminum oxide on the first insulating film;

forming a pixel electrode over the second insulating film, said pixel electrode electrically connected to the thin film transistor;

forming an EL layer over the pixel electrode;

forming a second electrode over the EL layer,

wherein the EL layer is selectively formed through an ink jet method.

3. A method for manufacturing an electrical device, said method comprising:

forming at least a thin film transistor on an insulating surface;

forming a first insulating film comprising an organic resin over the thin film transistor;

forming a second insulating film comprising diamond like carbon on the first insulating film;

forming a pixel electrode over the second insulating film, said pixel electrode electrically connected to the thin film transistor;

forming a EL layer over the pixel electrode;

forming a second electrode over the EL layer;

wherein the EL layer is selectively formed through an ink jet method.

4. A method for manufacturing an electrical device, said method comprising:

forming at least a thin film transistor on an insulating surface;

forming a first insulating film comprising silicon nitride over the thin film transistor;

forming a second insulating film comprising an organic resin on the first insulating film;

forming a third insulating film comprising silicon nitride on the second insulating film, wherein the third insulating film comprises the same material as the first insulating film;

forming a pixel electrode over the third insulating film, said pixel electrode electrically connected to the thin film transistor;

forming an EL layer over the pixel electrode;

forming a second electrode over the EL layer,

wherein the EL layer is selectively formed through an ink jet method.

5. A method for manufacturing an electrical device comprising:

forming at least a thin film transistor on an insulating surface;

forming a first insulating film comprising at least one selected from the group consisting of aluminum oxide, aluminum nitride and nitrated aluminum oxide over the thin film transistor;

forming a second insulating film comprising an organic resin on the first insulating film;

forming a third insulating film comprising at least the one selected from the group consisting of aluminum oxide, aluminum nitride and nitrated aluminum oxide on the second insulating film, wherein the third insulating film comprises the same material as the first insulating film;

forming a pixel electrode over the third insulating film, said pixel electrode electrically connected to the thin film transistor;

forming an EL layer over the pixel electrode;

forming a second electrode over the EL layer,

wherein the EL layer is selectively formed through an ink jet method.

8. A method according to claim 1, wherein the EL layer is an organic material.

9. A method according to claim 1, wherein the ink jet method uses a piezo element.

13. A method according to claim 2, wherein the EL layer is an organic material.

14. A method according to claim 2, wherein the ink jet method uses a piezo element.

15. A method according to claim 3, wherein the EL layer is an organic material.

16. A method according to claim 3, wherein the ink jet method uses a piezo element.

17. A method according to claim 4, wherein the EL layer is an organic material.

18. A method according to claim 4, wherein the ink jet method uses a piezo element.

19. A method according to claim 5, wherein the EL layer is an organic material.

20. A method according to claim 5, wherein the ink jet method uses a piezo element.

30. A method according to claim 1, wherein one of the pixel electrode and the second electrode comprises at least one selected from the group consisting of magnesium (Mg), lithium (Li), cesium (Cs), barium (Ba), potassium (K), beryllium (Be), or calcium (Ca).

31. A method according to claim 1, wherein the second insulating film comprises at least one selected from the group consisting of silicon nitride oxide and silicon nitride.

33. A method according to claim 2, wherein one of the pixel electrode and the second electrode comprises at least one selected from the group consisting of magnesium (Mg), lithium (Li), cesium (Cs), barium (Ba), potassium (K), beryllium (Be), or calcium (Ca).

34. A method according to claim 2, wherein the insulating film comprising aluminum nitride.

36. A method according to claim 3, wherein one of the pixel electrode and the second electrode comprises at least one selected from the group consisting of magnesium (Mg), lithium (Li), cesium (Cs), barium (Ba), potassium (K), beryllium (Be), or calcium (Ca).

37. A method according to claim 4, wherein one of the pixel electrode and the second electrode comprises at least one selected from the group consisting of magnesium (Mg), lithium (Li), cesium (Cs), barium (Ba), potassium (K), beryllium (Be), or calcium (Ca).

38. A method according to claim 4, wherein the EL layer is formed in a dry nitrogen atmosphere.

39. A method according to claim 5, wherein one of the pixel electrode and the second electrode comprises at least one selected from the group consisting of magnesium (Mg), lithium (Li), cesium (Cs), barium (Ba), potassium (K), beryllium (Be), or calcium (Ca).

40. A method according to claim 5, wherein the EL layer is formed in a dry argon atmosphere.

41. A method according to claim 1, further comprising:

forming a contact hole in the first and second insulating films,

wherein an upper diameter of the contact hole is longer length than a lower diameter of the contact hole.

42. A method according to claim 1, further comprising:

forming a contact hole in the first and second insulating films;

forming the pixel electrode on the second insulating film,

wherein the second insulating film is not in contact with side surfaces of the contact hole while the pixel electrode is in contact with the side surface of the contact hole and edges of the first and second insulating films.

43. A method according to claim 2, further comprising:

forming a contact hole in the first and second insulating films,

wherein an upper diameter of the contact hole is longer length than a lower diameter of the contact hole.

44. A method according to claim 2, further comprising:

forming a contact hole in the first and second insulating films;

forming the pixel electrode on the second insulating film,

wherein the second insulating film is not in contact with side surfaces of the contact hole while the pixel electrode is in contact with the side surface of the contact hole and edges of the first and second insulating films.

45. A method according to claim 3, further comprising:

forming a contact hole in the first and second insulating films,

wherein an upper diameter of the contact hole is longer length than a lower diameter of the contact hole.

46. A method according to claim 3, further comprising:

forming a contact hole in the first and second insulating films;

forming the pixel electrode on the second insulating film,

wherein the second insulating film is not in contact with side surfaces of the contact hole while the pixel electrode is in contact with the side surface of the contact hole and edges of the first and second insulating films.

47. A method according to claim 4,

wherein the third insulating film comprises at least one selected from the group consisting of silicon nitride oxide and silicon nitride.

48. A method according to claim 4, further comprising:

forming a contact hole in the first, second and third insulating films,

wherein an upper diameter of the contact hole is longer length than a lower diameter of the contact hole.

49. A method according to claim 4, further comprising:

forming a contact hole in the first, second and third insulating films;

forming the pixel electrode on the third insulating film,

wherein the third insulating film is not in contact with side surfaces of the contact hole while the pixel electrode is in contact with the side surface of the contact hole and edges of the first, second and third insulating films.

50. A method according to claim 5, further comprising:

forming a contact hole in the first, second and third insulating films,

wherein an upper diameter of the contact hole is longer length than a lower diameter of the contact hole.

51. A method according to claim 5, further comprising:

forming a contact hole in the first, second and third insulating films;

forming the pixel electrode on the third insulating film,

wherein the third insulating film is not in contact with side surfaces of the contact hole while the pixel electrode is in contact with the side surface of the contact hole and edges of the first, second and third insulating films.

52. A method for manufacturing an electrical device comprising:

forming at least a thin film transistor on an insulating surface;

forming a first insulating film comprising diamond like carbon over the thin film transistor;

forming a second insulating film comprising an organic resin on the first insulating film;

forming a third insulating film comprising diamond like carbon on the second insulating film, wherein the third insulating film comprises the same material as the first insulating film;

forming a pixel electrode over the third insulating film, said pixel electrode electrically connected to the thin film transistor;

forming an EL layer over the pixel electrode;

forming a second electrode over the EL layer,

wherein the EL layer is selectively formed through an ink jet method.

53. A method according to claim 52, wherein the EL layer is an organic material.

54. A method according to claim 52, wherein the ink jet method uses a piezo element.

55. A method according to claim 52, wherein one of the pixel electrode and the second electrode comprises at least one selected from the group consisting of magnesium (Mg), lithium (Li), cesium (Cs), barium (Ba), potassium (K), beryllium (Be), or calcium (Ca).

56. A method according to claim 52, further comprising:

forming a contact hole in the first, second and third insulating films,

wherein an upper diameter of the contact hole is longer length than a lower diameter of the contact hole.

57. A method according to claim 52, further comprising:

forming a contact hole in the first, second and third insulating films;

forming the pixel electrode on the third insulating film,

wherein the third insulating film is not in contact with side surfaces of the contact hole while the pixel electrode is in contact with the side surface of the contact hole and edges of the first, second and third insulating films.

58. A method for manufacturing an electrical device, said method comprising:

forming at least a thin film transistor on an insulating surface;

forming a first insulating film over the thin film transistor;

forming a second insulating film on the first insulating film;

forming a third insulating film on the second insulating film;

forming a fourth insulating film on the third insulating film;

forming a contact hole in the second, third and fourth insulating films;

forming a pixel electrode over the fourth insulating film, said pixel electrode electrically connected to the thin film transistor through the contact hole;

forming a bank on the fourth insulating film;

forming an EL layer over the pixel electrode;

forming a second electrode over the EL layer;

forming a protection electrode over the second electrode;

forming a fifth insulating film over the protection electrode;

wherein the EL layer is selectively formed through an ink jet method,

wherein the third insulating film comprises an organic material,

wherein the EL layer is formed in a dry nitrogen atmosphere.

59. A method according to claim 58, wherein the EL layer is an organic material.

60. A method according to claim 58, wherein the ink jet method uses a piezo element.

61. A method according to claim 58,

wherein one of the pixel electrode and the second electrode comprises at least one selected from the group consisting of magnesium (Mg), lithium (Li), cesium (Cs), barium (Ba), potassium (K), beryllium (Be), or calcium (Ca).

62. A method according to claim 58, wherein an upper diameter of the contact hole is longer length than a lower diameter of the contact hole.

63. A method according to claim 58, wherein the fourth insulating film is not in contact with side surfaces of the contact hole while the pixel electrode is in contact with the side surface of the contact hole and edges of the second, third and fourth insulating films.

64. A method according to claim 58, wherein each of second, fourth and fifth insulating films comprises a same material.

65. A method for manufacturing an electrical device, said method comprising:

forming at least a thin film transistor on an insulating surface;

forming a first insulating film over the thin film transistor;

forming a second insulating film on the first insulating film;

forming a third insulating film on the second insulating film;

forming a fourth insulating film on the third insulating film;

forming a contact hole in the second, third and fourth insulating films;

forming a pixel electrode over the fourth insulating film, said pixel electrode electrically connected to the thin film transistor through the contact hole;

forming a bank on the fourth insulating film;

forming an EL layer over the pixel electrode;

forming a second electrode over the EL layer;

forming a protection electrode over the second electrode;

forming a fifth insulating film over the protection electrode;

wherein the EL layer is selectively formed through an ink jet method,

wherein the third insulating film comprises an organic material,

wherein the EL layer is formed in a dry argon atmosphere.

66. A method according to claim 65, wherein the EL layer is an organic material.

67. A method according to claim 65, wherein the ink jet method uses a piezo element.

68. A method according to claim 65, wherein one of the pixel electrode and the second electrode comprises at least one selected from the group consisting of magnesium (Mg), lithium (Li), cesium (Cs), barium (Ba), potassium (K), beryllium (Be), or calcium (Ca).

69. A method according to claim 65, wherein an upper diameter of the contact hole is longer length than a lower diameter of the contact hole.

70. A method according to claim 65, wherein the fourth insulating film is not in contact with side surfaces of the contact hole while the pixel electrode is in contact with the side surface of the contact hole and edges of the second, third and fourth insulating films.

71. A method according to claim 65, wherein each of second, fourth and fifth insulating films comprises a same material.

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CLAIMS AS ALLOWED

59. An electroluminescence display device comprising:

a pixel portion and a peripheral driving circuit portion formed over a substrate;

at least a first thin film transistor for controlling current and a second thin film transistor for switching each being formed in the pixel portion;

at least a CMOS transistor formed in the peripheral driving circuit portion;

wherein the first thin film transistor includes:

a gate electrode having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with top and side surfaces of the first conductive layer and the gate insulating film;

a semiconductor layer comprising a first channel formation region, a first impurity region being in contact with the first channel formation region, and a second impurity region being in contact with the first impurity region;

a pixel electrode being electrically connected to the second impurity region of the first thin film transistor; and

a light emitting layer being formed over the pixel electrode,

wherein the first impurity region is disposed so as to completely overlaps with the second conductive layer with the gate insulating film interposed therebetween;

an electrode being formed over the light emitting layer.

60. An electroluminescence display device according to claim 59 wherein the light emitting layer is an EL layer.

61. An electroluminescence display device according to claim 59 wherein at least one of the pixel electrode and the electrode is transparent.

62. An electroluminescence display device according to claims 59 wherein a concentration of an impurity element for giving n-type in the first impurity region ranges from $1 \times 10^{16}$ atoms/cm$^3$ to $5 \times 10^{19}$ atoms/cm$^3$.

63. An electroluminescence display device according to claims 59 wherein the first

conductive layer of the first thin film transistor comprises one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprises a material containing those elements as ingredients.

64. An electroluminescence display device according to claims 59 wherein the first conductive layer of the first thin film transistor comprises a single layer or a plurality of layers.

65. An electroluminescence display device according to claims 59 wherein the first conductive layer of the first thin film transistor comprises at least:

a conductive layer (A) formed to come in contact with the gate insulating film, and comprising one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprising a material containing those elements as ingredients; and

a conductive layer (B) formed on the conductive layer (A), and comprising one or more kinds of elements selected from aluminum (Al) and copper (Cu), or comprising a material containing those elements as ingredients.

66. An electroluminescence display device according to claims 59 wherein the second conductive layer comprises one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprises a material containing those elements as ingredients.

67. An electroluminescence display device according to claims 59 wherein the electroluminescence display device is incorporated into an electronic equipment selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital versatile disk player, a goggle type display, an electronic game machine, and a projector.

68 . An electroluminescence display device comprising:

a pixel portion and a peripheral driving circuit portion formed over a substrate;

at least a first thin film transistor for controlling current and a second thin film transistor for switching each being formed in the pixel portion;

at least a CMOS transistor formed in the peripheral driving circuit portion;

wherein the first thin film transistor includes:

a gate electrode having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with top and side surfaces of the first conductive layer and the gate insulating film;

a semiconductor layer comprising a first channel formation region, a first impurity region being in contact with the first channel formation region, and a second impurity region being in contact with the first impurity region;

a pixel electrode being electrically connected to the second impurity region of the first thin film transistor; and

a light emitting layer being formed over the pixel electrode,

wherein the first impurity region is disposed so as to partially overlaps with the second conductive layer with the gate insulating film interposed therebetween,

an electrode being formed over the light emitting layer.

69 . An electroluminescence display device according to claim 68 wherein the light emitting layer is an EL layer.

70 . An electroluminescence display device according to claim 68 wherein at least one of the pixel electrode and the electrode is transparent.

71 . An electroluminescence display device according to claims 68 wherein a concentration of an impurity element for giving n-type in the first impurity region ranges from $1 \times 10^{16}$ atoms/cm$^3$ to $5 \times 10^{19}$ atoms/cm$^3$.

72 . An electroluminescence display device according to claims 68 wherein the first conductive layer of the first thin film transistor comprises one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprises a material containing those elements as ingredients.

73 . An electroluminescence display device according to claims 68 wherein the first conductive layer of the first thin film transistor comprises a single layer or a plurality of layers.

74 . An electroluminescence display device according to claims 68 wherein the first conductive layer of the first thin film transistor comprises at least:

a conductive layer (A) formed to come in contact with the gate insulating film, and comprising one or more kinds of elements selected from a group consisting of titanium (Ti),

tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprising a material containing those elements as ingredients; and

a conductive layer (B) formed on the conductive layer (A), and comprising one or more kinds of elements selected from aluminum (Al) and copper (Cu), or comprising a material containing those elements as ingredients.

75 . An electroluminescence display device according to claims 68 wherein the second conductive layer comprises one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprises a material containing those elements as ingredients.

76 . An electroluminescence display device according to claims 68 wherein the electroluminescence display device is incorporated into an electronic equipment selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital versatile disk player, a goggle type display, an electronic game machine, and a projector.

77 . An electroluminescence display device comprising:

a pixel portion and a peripheral driving circuit portion formed over a substrate;

at least a first thin film transistor for controlling current and a second thin film transistor for switching each being formed in the pixel portion;

at least a CMOS transistor formed in the peripheral driving circuit portion;

wherein each of the first thin film transistor and the second thin film transistor includes:

a gate electrode having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with top and side surfaces of the first conductive layer and the gate insulating film;

a semiconductor layer comprising a first channel formation region, a first impurity region being in contact with the first channel formation region, and a second impurity region being in contact with the first impurity region,

wherein the first impurity region is disposed so as to completely overlaps with the second conductive layer with the gate insulating film interposed therebetween in at least one of the first thin film transistor and the second thin film transistor;

wherein a pixel electrode is electrically connected to the second impurity region of the first thin film transistor,

wherein a light emitting layer is formed over the pixel electrode,

wherein an electrode is formed over the light emitting layer.

78 . An electroluminescence display device according to claim 77 wherein the light emitting layer is an EL layer.

79 . An electroluminescence display device according to claim 77 wherein at least one of the pixel electrode and the electrode is transparent.

80 . An electroluminescence display device according to claims 77 wherein a concentration of an impurity element for giving n-type in the first impurity region ranges from $1 \times 10^{16}$ atoms/cm$^3$ to $5 \times 10^{19}$ atoms/cm$^3$.

81 . An electroluminescence display device according to claims 77 wherein the first conductive layer of the first thin film transistor comprises one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprises a material containing those elements as ingredients.

82 . An electroluminescence display device according to claims 77 wherein the first conductive layer of the first thin film transistor comprises a single layer or a plurality of layers.

83 . An electroluminescence display device according to claims 77 wherein the first conductive layer of the first thin film transistor comprises at least:

a conductive layer (A) formed to come in contact with the gate insulating film, and comprising one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprising a material containing those elements as ingredients; and

a conductive layer (B) formed on the conductive layer (A), and comprising one or more kinds of elements selected from aluminum (Al) and copper (Cu), or comprising a material containing those elements as ingredients.

84 . An electroluminescence display device according to claims 77 wherein the second conductive layer comprises one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprises a material containing those elements as ingredients.

85 . An electroluminescence display device according to claims 77 wherein the electroluminescence display device is incorporated into an electronic equipment selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital versatile disk player, a goggle type display, an electronic game machine, and a projector.

86 . An electroluminescence display device comprising:

a pixel portion and a peripheral driving circuit portion formed over a substrate;

at least a first thin film transistor for controlling current and a second thin film transistor for switching each being formed in the pixel portion;

at least a CMOS transistor formed in the peripheral driving circuit portion;

wherein each of the first thin film transistor and the second thin film transistor includes:

a gate electrode having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with top and side surfaces of the first conductive layer and the gate insulating film;

a semiconductor layer comprising a first channel formation region, a first impurity region being in contact with the first channel formation region, and a second impurity region being in contact with the first impurity region,

wherein the first impurity region is disposed so as to completely overlaps with the second conductive layer with the gate insulating film interposed therebetween in at least one of the first thin film transistor and the second thin film transistor;

wherein a pixel electrode is electrically connected to the second impurity region of the first thin film transistor,

wherein a light emitting layer is formed over the pixel electrode,

wherein an electrode is formed over the light emitting layer.

87 . An electroluminescence display device according to claim 86 wherein the light emitting layer is an EL layer.

88 . An electroluminescence display device according to claim 86 wherein at least one of the pixel electrode and the electrode is transparent.

89 . An electroluminescence display device according to claims 86 wherein a concentration of an impurity element for giving n-type in the first impurity region ranges from

$1 \times 10^{16}$ atoms/cm$^3$ to $5 \times 10^{19}$ atoms/cm$^3$.

90 . An electroluminescence display device according to claims 86 wherein the first conductive layer of the first thin film transistor comprises one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprises a material containing those elements as ingredients.

91 . An electroluminescence display device according to claims 86 wherein the first conductive layer of the first thin film transistor comprises a single layer or a plurality of layers.

92 . An electroluminescence display device according to claims 86 wherein the first conductive layer of the first thin film transistor comprises at least:

a conductive layer (A) formed to come in contact with the gate insulating film, and comprising one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprising a material containing those elements as ingredients; and

a conductive layer (B) formed on the conductive layer (A), and comprising one or more kinds of elements selected from aluminum (Al) and copper (Cu), or comprising a material containing those elements as ingredients.

93 . An electroluminescence display device according to claims 86 wherein the second conductive layer comprises one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprises a material containing those elements as ingredients.

94 . An electroluminescence display device according to claims 86 wherein the electroluminescence display device is incorporated into an electronic equipment selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital versatile disk player, a goggle type display, an electronic game machine, and a projector.

95 . An electroluminescence display device comprising:

a pixel portion and a peripheral driving circuit portion formed over a substrate;

at least a first thin film transistor for controlling current and a second thin film transistor for switching each being formed in the pixel portion;

at least a CMOS transistor formed in the peripheral driving circuit portion;

wherein the first thin film transistor includes:

a gate electrode having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with top and side surfaces of the first conductive layer and the gate insulating film;

a semiconductor layer comprising a first channel formation region, a first impurity region being in contact with the first channel formation region, and a second impurity region being in contact with the first impurity region;

a pixel electrode being electrically connected to the second impurity region of the first thin film transistor; and

wherein the first impurity region is disposed so as to completely overlaps with the second conductive layer with the gate insulating film interposed therebetween;

wherein a light emitting layer is formed over the pixel electrode,

wherein an electrode is formed over the light emitting layer,

wherein the first thin film transistor has a p-type conductivity.

96 . An electroluminescence display device according to claim 95 wherein the light emitting layer is an EL layer.

97 . An electroluminescence display device according to claim 95 wherein at least one of the pixel electrode and the electrode is transparent.

98 . An electroluminescence display device according to claims 95 wherein the first conductive layer of the first thin film transistor comprises one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprises a material containing those elements as ingredients.

99 . An electroluminescence display device according to claims 95 wherein the first conductive layer of the first thin film transistor comprises a single layer or a plurality of layers.

100 . An electroluminescence display device according to claims 95 wherein the first conductive layer of the first thin film transistor comprises at least:

a conductive layer (A) formed to come in contact with the gate insulating film, and

comprising one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprising a material containing those elements as ingredients; and

a conductive layer (B) formed on the conductive layer (A), and comprising one or more kinds of elements selected from aluminum (Al) and copper (Cu), or comprising a material containing those elements as ingredients.

101 . An electroluminescence display device according to claims 95 wherein the second conductive layer comprises one or more kinds of elements selected from a group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo), or comprises a material containing those elements as ingredients.

102 . An electroluminescence display device according to claims 95 wherein the electroluminescence display device is incorporated into an electronic equipment selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital versatile disk player, a goggle type display, an electronic game machine, and a projector.